Non destructive control of flip chip packages for space applications

Abstract

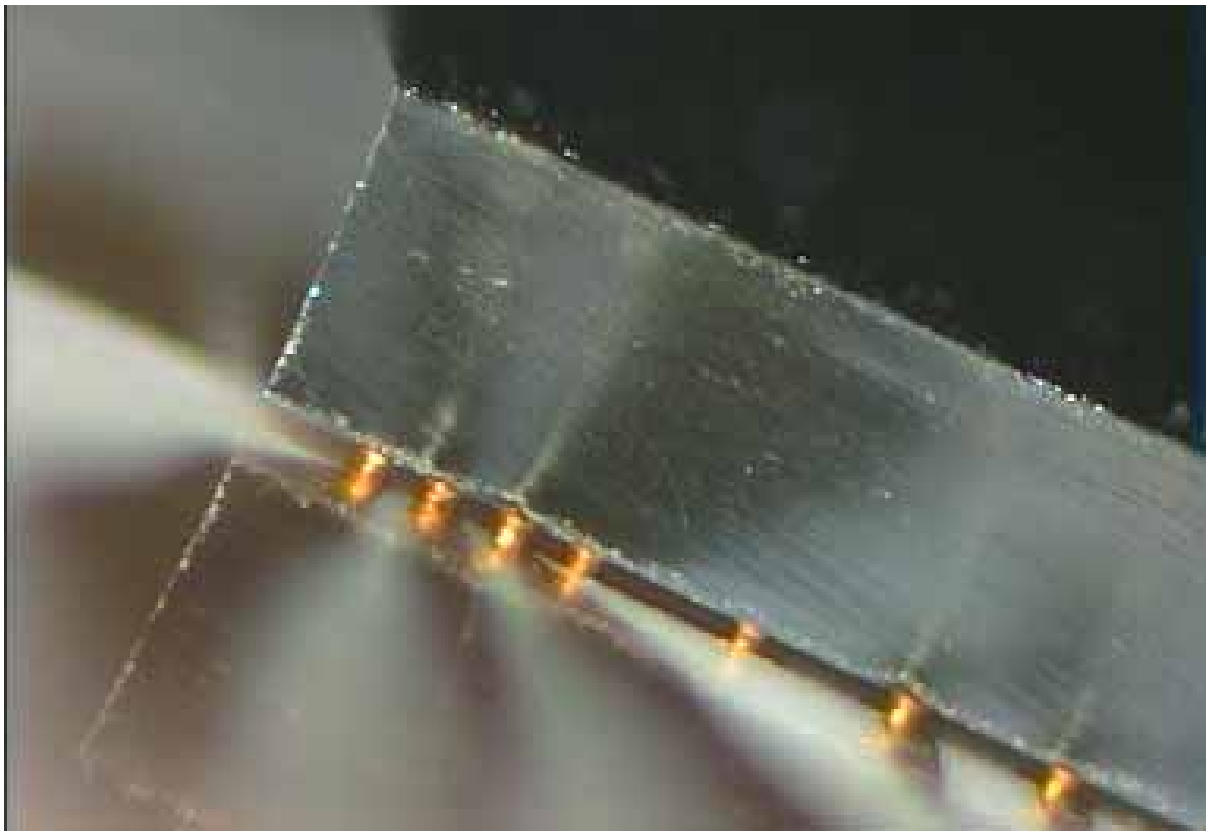
Shrinking dimensions of flip chip assemblies make inspection of bumps or solder joints always more difficult as standard non destructive control techniques reach their resolution limits. This issue is particularly critical for RF flip chip assemblies manufactured at Alcatel Space with stud bumps as small as a few tens of micrometers regarding quality requirements from space industry. In this paper, non destructive control of flip chip packages is addressed by 3D-Electronic Speckles Pattern Interferometry (3D-ESPI). This original non contact and full field technique allows deformation measurements of microsystems with a sub-micron resolution and was successfully applied to detect defaults such as missing bumps in flip chip assemblies.

Introduction

Flip chip is an interconnection technology where a face-down (or "flipped") electronic components is both mechanically and electrically connected to its substrate in a one step process by means of bumps or solder joints.

This technology offers major improvements over the standard wire bonding technique, especially in terms of number of Inputs/Outputs (I/O), components density and electrical performances at high frequency. Hence flip chip packaging is getting more and more popular in microelectronics industry.

For flip chip, the continuous trend for higher number of I/O and finer pitch translates into higher number of smaller bumps. This makes reliability of flip chip assemblies more and more difficult to achieve both during their manufacturing process and at the component lifetime scale. And with reliability comes another issue: inspection of interconnections as bumps are hidden below the die, preventing visual inspection as for wire bonding. As a consequence, identification of defaults and failure modes in flip chip assemblies required Non Destructive Control (NDC) techniques able to detect very small features such as cracks in a bump, delamination at the bump/chip or bump/substrate interface…



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Several NDC techniques such as X-Ray microscopy [1] Infrared Thermography or Scanning Acoustic Microscopy have been used to this purpose and can offer significant results for inspection of Ball Grid Array (BGA) or flip chip assemblies with rather large bumps (i.e. >100 µm). However, these methods reach their resolution limits for inspection of packages with bumps as small as a few tens of microns. To overcome this limitation, NDC techniques based on optical interferometry with submicron resolution have recently been proposed such as Moiré [2], laser ultrasound coupled to interferometry [3] or Electronic Speckle Pattern Interferometry described hereafter.

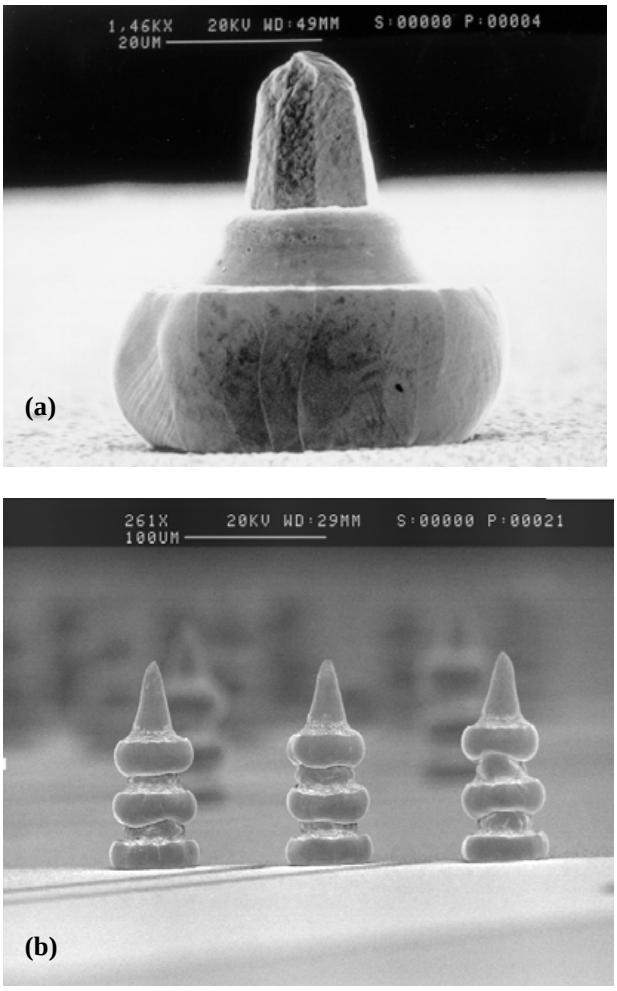

Fig 1: Simple (a) and triple stacked (b) stub bumps.

Flip Chip at Alcatel Space

Flip chip assemblies manufactured at Alcatel Space are dedicated to RF applications. Hence, parts to be connected are mainly GaAs Monolithic Microwave Integrated Circuits (MMIC) and ceramic substrates both with gold pads. For that reason, the technology chosen to make flip chip assemblies is thermocompression with gold stud bumps [4]. Gold stud bumps are made on the substrate thanks to a modified "ball bonding" process (Fig. 1a). Depending on RF applications, bumps can be stacked in order to obtain double or even triple bumps (see Fig. 1b). MMICs are then connected to the substrate by thermocompression with a flip chip bonder providing the temperature and pressure required to make the assembly. An example of such an assembly is given Fig. 2. This technique offers the advantage to allow the use of MMIC off the shelves without any extra process at the wafer level and is also compatible with many ceramic substrates (AlN, Alumina..). These flip chip assemblies based on stud bumps and developed for RF purposes exhibit several specificities compared to the ones based on solder balls arrays and commonly encountered in digital electronics. First, gold stud bumps are very small: their diameter is limited to 50 µm whereas their height is in the 20 to 80 µm range depending on the number of stacked bumps (see Fig. 1). Then the number of bumps per chip is very limited: 10 to 20 bumps are often enough to connect all the RF access and DC pads. And finally, bumps are mainly located at the die periphery.

Non destructive control of Flip Chip assemblies

In space industry, quality standards require a systematic visual inspection of connections in hybrids packages. If control does not rise any problem for wire bonding, it becomes a critical issue for flip chip assemblies where bumps performing both electrical and mechanical connections are hidden by the die itself. Then, visual inspection has to be replaced by other Non Destructive Control techniques. The challenge for flip chip packages manufactured at Alcatel Space deals with the very small size of stud bumps to be inspected.
Several techniques were evaluated at Alcatel Space to perform NDC on our flip chip assemblies but the most standard ones were shown to reach their resolution limits. Images obtained by Infrared Thermography for example are affected by all the metal layers deposited at the die surface.

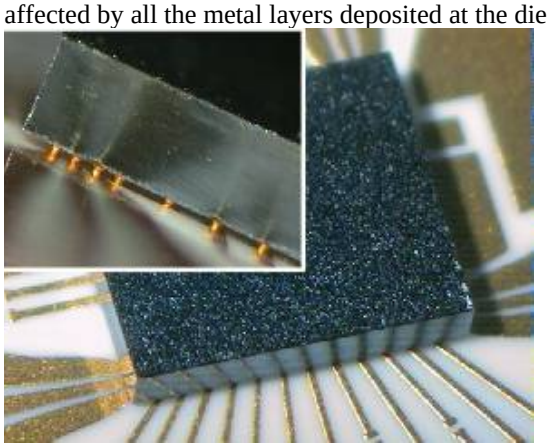

Fig. 2: Top and side (inset) view of a flip chip assembly.

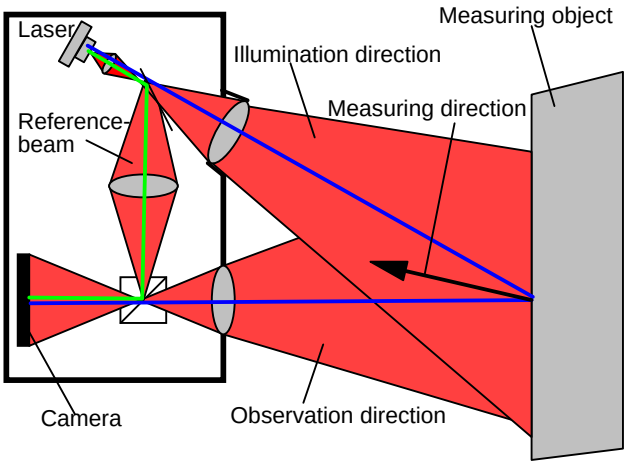

Fig. 3: Basic principle of an ESPI set-up

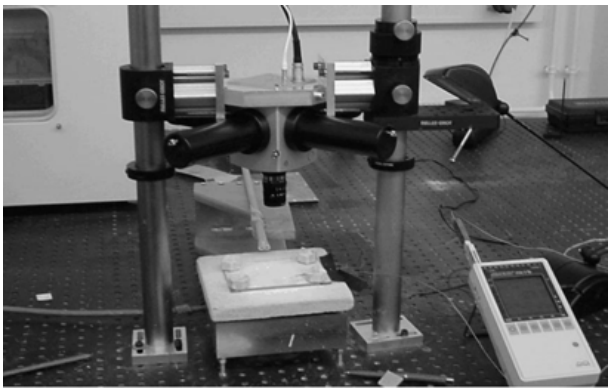

Fig. 4: 3D-ESPI set-up

In particular, bumps pads prevent to have a clear picture of bumps themselves. Scanning Acoustic Microscopy was also tested but without success as a trade off has to be made between resolution and penetration depth of the ultrasound into the package. And finally recent X-Ray microscopy set up have allowed the detection of small bumps below the die but without the resolution to identify any defect at the bump level. Moreover, in our particular case with stud bumps located at the die periphery, resolution from these last two methods suffers from edge effects.
3D-Electronic Speckles Pattern Interferometry (3D-ESPI) is an original alternative NDC technique for microsystems inspection [5]. This full field measurement method enables three dimensional deformation analysis of any component without contact and with a sub-micron resolution.
ESPI measurements are performed by illuminating the device under test with laser light as depicted on Fig. 3. Lightwaves reflected by every single point from the object surface interfere and create a so-called speckle pattern recorded by a CCD camera and stored as a reference. When a stress such as heating is applied, the object surface moves and the speckle pattern is modified. From the comparison of this new pattern with the reference one, correlation fringes representing the displacement of the object surface are deduced. Finally, software analysis of these fringes allows to compute the quantitative strain experienced by the inspected device.
In practice, to measure displacements of the device under test in both the two in plane directions and the out of plane one, four illumination directions are used in the real 3-D ESPI set-up illustrated Fig. 4. To prevent any vibration artefact during acquisition, the whole set-up is also mounted on an air cushion table.
Applied to Flip Chip packages inspection, 3D-ESPI measurements are expected to detect different deformations behaviour between assemblies with and without defaults such as missing bumps, open connections or cracks….

3D-ESPI measurements on Flip Chip Assemblies

Flip chip samples were manufactured with 4x5.5mm², 100 µm thin, GaAs MMICs connected to AlN substrates (see Fig. 5). Chips used in this experiment are test devices with daisy chains to allow electrical control of every connection. Hence assemblies exhibit a large number (up to 130) of double stud bumps located both in the middle of the chip and at its periphery.
Two groups of samples were prepared. The first one is composed of assemblies with all their 130 bumps. The second group consists of flip chip assemblies with defects. In order to evaluate the 3D-ESPI system sensitivity in the first phase of this work, "large" defaults were intentionally introduced and half of the bumps were removed. Then all the remaining bumps were located at the die periphery.
In both cases, resistance measurements were performed on daisy chains and indicated that all the contacts were electrically correct both after the flip chip bonding process and after ESPI measurements.

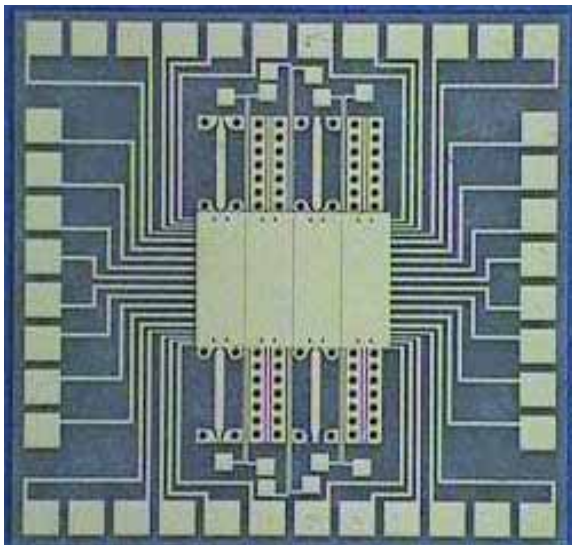

Fig. 5: Flip chip assembly (GaAs die connected on AlN substrate) for 3D ESPI measurements

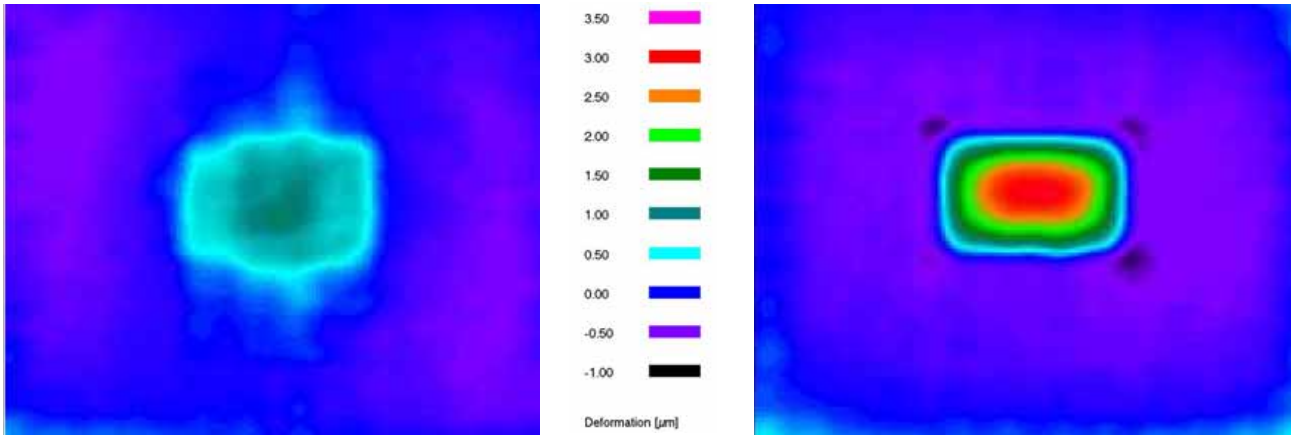

Fig. 6(a): 3D-ESPI out of plane displacement measured between 25°C and 125°C on the assembly from fig. 5 the die is connected with all its bumps. (b): Same measurement for a die with only half of its bumps. The grey scale indicating the z-displacement is the same on both figures.

3D-ESPI measurements were performed between room temperature and 125 C. Images of the speckle pattern were recorded every 5 C and deformations of the flip chip packages in the three directions were deduced.
Fig. 6a represents the computed out of plane displacement (or z-deformation) experienced by a chip with all its bumps: 0.5 micron z-deformation is observed at the center of the die (with a repeatability of 0.1 µm between several measurements).
As resistance measurements performed on daisy chains have indicated that all the contacts were electrically correct on this die before and after ESPI measurements, the observed strain can be attributed only to the small coefficient of thermal expansion (CTE) mismatch between the GaAs die (CTE ~ 6 ppm/ C) and the AlN substrate (CTE ~ 4 ppm/ C).
Fig. 6b exhibits the results of the same measurement performed on a die where half of the bumps were removed. Here the z-deformation at the centre of the die is higher than 3 microns! The large difference between these two measurements is summarised on Fig. 7 with the illustration of the out of plane displacement of both packages along their diagonal. This result clearly indicates that the 3D-ESPI techniques could detect defaults such as missing bumps in flip chip assemblies.

Discussion

Further experiments are currently performed on more representative MMICs (i.e. with less bumps) to evaluate the detection limit of the ESPI set-up regarding the nature of the default to be detected. The ultimate objective of this work is indeed to identify defects such as cracks or delamination at the single bump level.
Influence of materials involved in the assemblies is also under investigation as CTE mismatch between die and substrate has a direct influence on the deformation to be measured. One of the limitations of the ESPI technique could be the difficulty to detect any deformation on flip chip assemblies where CTE of the die and substrate are matched together, as GaAs on alumina for example. On the opposite, it should be much easier to analyse flip chip packages with solder joints on organic substrate which exhibits large CTE mismatch.
Beyond the results presented here about flip chip inspection, 3D-ESPI is also a powerful technique to perform material characterisation (CTE or Young modulus measurements for example) or residual stress analysis. Thus it could be a useful complementary tool to thermo-mechanical simulations to improve the reliability of electronic packages and microsystems (BGA, MEMS…).

Conclusion

Non destructive control of flip chip assemblies with very small (~ 50 microns) stud bumps was successfully performed by 3D-Electronic Speckles Pattern Interferometry measurements. This method allows measurements of in plane and out of plane displacement of component submitted to thermal loading, and differences in behaviour of good die and dies with defaults such as missing were shown to be detectable.

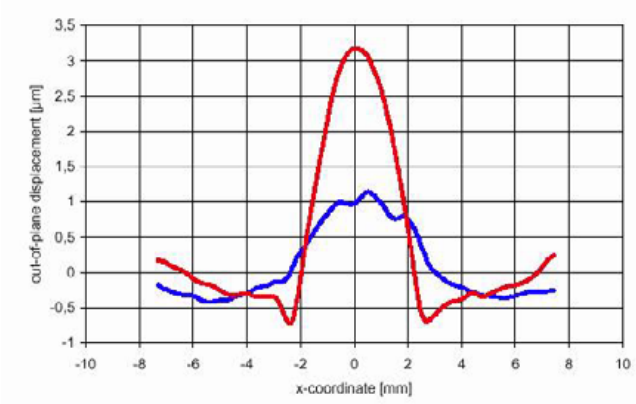

Fig. 7: Out of plane displacement in the diagonal of flip chip assemblies with (soft grey) and without (dark

Acknowledgements

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